REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-23 in the application. Previously, the Applicant amended Claims 1, 4, 9, 12, 17 and 20 and canceled Claims 5, 13 and 21 without prejudice or disclaimer.

In the present response, the Applicant has amended Claims 1, 4, 6-7, 9, 12, 14-15, 17, 20 and 22-23 and added Claims 24-25. Support for the amended claims can be found in paragraphs 57-60 and Figure 3 of the original specification. Accordingly, Claims 1-4, 6-12, 14-20 and 22-25 are currently pending in the application.

I. Rejection of Claims 1-4 and 6-23 under 35 U.S.C. §102

The Examiner rejected Claims 1-4 and 6-23 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,498,136 to Sproul, III. The Applicant respectfully disagrees in view of amended independent Claims 1, 9 and 17.

Sproul is directed to an interrupt controller for an instruction pipelined digital processor. (*See* column 1, lines 6-9.) Sproul discloses an interrupt processor for a pipeline that includes a return address generator pipeline having a sequence of staging registers and associated logic. (*See* column 4, lines 38-40 and Figure 1.) The interrupt processor also includes a stack register that stores a program counter value input from the return address generator pipeline. This program counter value is the value to which the instruction pipeline is to return after an interrupt operation is complete. (*See* column 5, lines 42-51 and Figures 1-2.)

Sproul does not teach, among other things, generating multiple return PC values for call instructions in a pipeline of a processor, storing the return PC values in a PC queue of a return PC

storage and making one of the return PC values available to a PC of a processor upon execution of a corresponding return instruction by employing staging registers to track the corresponding return instruction while moving through stages in a pipeline as recited in independent Claims 1, 9 and 17. On the contrary, Sproul teaches sequentially propagating a program count indicator to output lines of the return address generator pipeline. The stack register, in response to the program count indicator, stores the program counter value for the instruction pipeline. (*See* column 4, lines 47-56 and Figures 1-2.) Thus, Sproul discloses propagating a program count indicator that is input to the stack register for the stack register to use to determine a program counter value to store. Sproul provides no teaching, however, of storing **multiple return PC values** in a PC queue or **making one** of the return PC values from the PC queue **available for a PC by employing staging registers for tracking** as presently claimed. Sproul, therefore, does not teach each element of amended independent Claims 1, 9 and 17.

Since Sproul does not disclose each element of independent Claims 1, 9 and 17, Sproul does not anticipate Claims 1, 9 and 17 and Claims dependent thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 1-4, 6-12, 14-20 and 22-25 and allow issuance thereof.

II. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-4, 6-12, 14-20 and 22-25.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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